REMARKS

In the Office Action, the Examiner rejected claims 1-44. By this paper, claims 1-3, 16-17, 19, 25, 31-32, 35-36, 40-42 and 44 have been amended to clarify the subject matter claimed. Applicants respectfully request reconsideration and allowance of all pending claims.

Claim Rejections under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 1-44 under U.S.C. § 102(e) as being unpatentable over Bashford (U.S. Patent No. 6,629,179, hereafter "the Bashford reference"). Applicants respectfully traverse this rejection.

Legal Precedent

Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

Claims 1-44

In the present case, the Bashford reference fails to anticipate Applicants' claims, because every element of the claimed invention is not shown in the Bashford reference. Specifically, independent claims 1 and 19 recite "a first counter; and a second counter, the first and second counters adapted to increment whenever an entry is enqueued or dequeued from the first circular queue." Independent claim 36 recites "incrementing a first counter and a second counter whenever an entry is enqueued to or dequeued from the first circular queue." Independent claim 40 recites "means for incrementing a counting means whenever an entry is enqueued to or dequeued from the first queue means."

In contrast, the Bashford reference discloses a system where the first and second counters are associated with two different queues. To be clear, the Examiner cited to the posted write registers 404 as a first circular queue, the circular queue 408 as a second circular queue, the posted write tracking circuitry 412 as a first counter and the interrupt pointer of the circular queue as a second counter. Office action, pg 2, lines 23-28 and pg 3, lines 3-14. The posted write tracking circuitry 412 is coupled with the posted write registers and transmits a decrement signal to the posted write registers 404 whenever write data is posted from the PCI bridge. Bashford, col. 8, lines 14-19. The interrupt pointer of the circular queue 408, however, is incremented according to entries in the circular queue and is not associated with the posted write registers 404. *See,* Bashford, col. 8, lines 50-53. Specifically, the incoming interrupt pointer in the circular queue 408 is incremented after an interrupt bit number has been entered into the circular queue 408 itself, not the posted write registers 404. *See*, col. 8, lines 29-35. As explained in the Bashford reference:

> When an interrupt needs to be entered into the circular queue 408 the interrupting bit number is entered, in operation 704, into the queue 408 at the location pointed to by an incoming_interrupt pointer in the queue 408. After the interrupt bit number has been entered, the incoming_interrupt pointer is incremented to point to the next location in the circular queue 408 in operation 706.

Col.8, lines 29-35.

> When interrupt bit number has been stored, the circular queue 408 increments the incoming interrupt register 836 to point to the next register in the circular chain of registers 802 to 832. In this manner, incoming interrupt bit numbers are queued in order.

Col 8, lines 50-53.

In other words, the pointer in the circular queue 408 is incrementing as a result of having received and entered an interrupt bit number *into the circular queue itself.* Therefore, the incrementing of the interrupt pointer and the posted write tracking circuitry 412 in the Bashford reference are not based on the enqueuing or dequeuing of entries in a common queue as set forth in the present claims.

Furthermore, independent claims 1, 19 and 36 all recite a "first circular queue" and a "second circular queue." These claim features, however, are absent from the Bashford reference. In the Office Action, the Examiner cited to the posted write registers 404 in the Bashford reference as a "first circular queue" and the circular queue 408 as a "second circular queue." However, the posted write registers 404 *are not a circular queue.* The posted write registers 404 are a series of registers each storing the number of posted writes pending for a corresponding interrupt bit number. *See*, col. 7, lines 65-67. The number of posted write registers is equal to the number of interrupt bits in the interrupt register. *See*, col. 8, lines 4-6. Whenever write data is posted to the PCI bus a decrement signal is sent to the posted write register 404 and all posted write registers with a non-zero value are decremented. *See*, col. 8,

lines 14-19. As such, the posted write registers 404 are not circular, but rather linear because each corresponds to an interrupt bit and holds the number of posted writes to be completed prior to generating an interrupt message over the PCI bus. *See*, col. 8, lines 18-22.

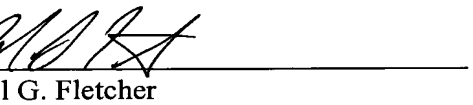
As such, for at least the reasons stated above, Applicants respectfully submit that independent claims 1, 19, 36 and 40, and thus all claims dependent thereon, are not anticipated by the Bashford reference. Accordingly, Applicants respectfully request Examiner withdraw the rejection of claims 1-44.

Conclusion

Applicants respectfully submit that all pending claims should be in condition for allowance. However, if the Examiner wishes to resolve any other issues by way of a telephone conference, the Examiner is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Date: September 22, 2005



Michael G. Fletcher
Reg. No. 32,777
(281) 970-4545

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400